REMARKS/ARGUMENT

Claims 1-10, 16-23 and 25 stand allowed.

Claims 11-15 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fourtet (US 6,345,173). Applicants respectfully traverse this rejection, as set forth below.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 11, as amended, requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock", "a **digital** direct modulator operational in response to a **digital** modulating data signal and a phase error to generate the OTW" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the digital modulating data signal to generate the phase error**".

Independent Claim 12, as amended, requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock, the digitally-controlled oscillator comprising a voltage controlled oscillator and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW", "a **digital** direct modulator operational in response to a **digital** modulating data signal and a filtered phase error to generate the OTW" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the digital modulating data signal to generate the**

Independent Claim 13, as amended, requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock", "a **digital** direct modulator operational in response to a **digital** modulating data signal and a filtered phase error to generate the OTW, said direct modulator comprising a combinational element feeding the digitally controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the digital modulating data signal to generate the filtered phase error**".

Independent Claim 14, as amended, requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock", "a **digital** direct modulator operational in response to a **digital** modulating data signal and a filtered phase error to generate the OTW", "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the digital modulating data signal to generate the filtered phase error**" and "a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL".

In contrast, the circuit disclosed by Fourtet comprises two PLL-based frequency synthesizers: "main synthesizer" (152, 252) and "auxiliary synthesizer" (155, 255). The main synthesizer is used as a "reference signal generator" (154, 254), whereas the auxiliary synthesizer is used as a "frequency modulator" (150, 250). The principle of operation of the frequency modulator is to apply the modulation data signal to the VCO of the main synthesizer and also to the reference signal with the correct balance between the two paths.

Further, Fourtet uses the auxiliary PLL-based synthesizer to create the frequency-modulated reference signal, Fr, by the modulating data 151. This Fr signal is then used as a frequency reference input of the main PLL-based synthesizer. While it is the main

PLL in Fourtet which is responsive to the channel selection signal, it is the auxiliary PLL in Fourtet, not the main PLL, which is responsive to the modulating data signal. Further, considering the second feed of the modulating data 151, it should be clarified that it is the VCO 160, not the PLL-based frequency synthesizer 150 that is responsive to the modulating data 151.

Moreover, Claims 11-14, as amended, specifically recite that the direct modulator is DIGITAL – not analog. In contrast, Fourtet discloses that digital signal 151 **becomes** analog after the gain block 166 (with possible DAC operation there). The modulation data is converted into the frequency information (continuous-time domain, not the desired discrete or digital domain) of the reference signal Fr. Accordingly, there is no way that Fourtet discloses a fully-digital implementation of architecture of Fig. 3. Similarly, in Fig. 4, the digital modulation data 251 is converted into the frequency deviation (continuous-time domain, not the desired discrete or digital domain) of the reference clock Fr. The digital nature of the "digital direct modulator" that generates "the OTW" is thus not preserved.

Accordingly, to the extent Fourtet discloses a modulator, it is not a digital direct modulator. Similarly, to the extent Fourtet discloses any modulating data signal, it is not digital along the path. In contrast, the present invention requires "a **digital direct** modulator operational in response to **a channel selection signal AND the DIGITAL modulating data signal to generate the filtered phase error**". Accordingly, Fourtet fails to teach or suggest the second element of independent Claims 11-14. Moreover, Fourtet fails to teach or suggest the third element of independent Claims 11-14: "**a phase-**

-cked loop ... channel selection signal ... and the

DIGITAL modulating data signal to generate the filtered phase error".

Accordingly, the 35 U.S.C. 103(a) rejection of Claims 11-14 is overcome.

Claims 15 and 24 stand allowable as depending from allowable claims and including further limitation not taught or suggested by the references of record.

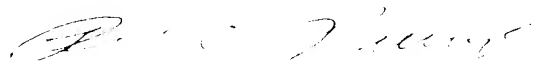
Claim 15 further defines the phase-locked loop system according to claim 14 wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator. The Fourtet reference fails to teach or suggest this additional requirement in combination with the previously discussed requirements of Claim 14.

Claim 24 further defines the phase-locked loop system according to claim 11 wherein said phase error is a filtered phase error. The Fourtet reference fails to teach or suggest this additional requirement in combination with the previously discussed requirements of Claim 11.

An amendment after a final rejection should be entered when it will place the case either in condition for allowance or in better form for appeal. 37 C.F.R. 1.116; MPEP 714.12. This amendment places the case in condition for allowance.

Claims 1-10, 16-23 and 25 stand allowed. Claims 11-16 and 24 stand allowable over the cited art and the application is in allowable form. By this amendment Claims 11-16 and 24 have been amended to be allowable over the cited reference. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4417